REMARKS

Claims 1-58 are pending in the application, with claims 1, 11, 21, 32, 43, 47, 51 and 55 being independent.

The specification has been amended to correct a translation error and for consistency with Fig. 2 of the application, which shows a connection between the source signal line 201 and one of a source region and a drain region of the active layer 206 through the connecting wiring 209. No new matter has been added.

Initially, applicant notes that, though the office action summary indicates that claims 1-58 have been rejected, actual rejections have only been provided for claims 1-20 and 43-58.

Claims 1, 2, 11, 12, 43, 44, 46-48, 50 and 51 have been rejected as being anticipated by Hirabayashi. With respect to claim 1 and its dependent claims, applicant requests reconsideration and withdrawal of the rejection because Hirabayashi does not describe or suggest "a semiconductor layer formed so as to be in contact with the planarization insulating film," as recited in claim 1. The action indicates that formation of such a semiconductor layer may be found in Hirabayashi at col. 4, lines 60-65. However, that passage and the subsequent text at col. 4, line 66 to col. 5, line 2, as well as Fig. 5(g), states that a single-crystal silicon substrate 20 is bonded to the insulating layer 5, and that the substrate 20 is separated from the insulating layer 5 by an oxide layer 3. Thus, the substrate 20 is not in contact with the insulating film 5. Accordingly, the rejection of claim 1 and its dependent claims should be withdrawn.

Similarly to claim 1, independent claim 11 recites a planarization insulating film on which a thin film transistor is formed so as to be in contact with the insulating film. As Hirabayashi nowhere describes or suggests such an arrangement, and the action nowhere alleges that Hirabayashi does, the rejection of claim 11 and its dependent claims should be withdrawn.

Similarly to claim 1, independent claims 43 and 47 recite forming a semiconductor layer (claim 43) or a thin film transistor (claim 47) such that the semiconductor layer or the thin film transistor is in contact with a planarization insulating film. Accordingly, applicant requests reconsideration and withdrawal of the rejection of claims 43 and 47, as well as their dependent claims, for the reasons discussed above with respect to claim 1.

Similarly to claim 1, independent claim 51 recites forming a capacitance wiring such that it is in contact with a planarization insulating film. Hirabayashi nowhere describes or suggests such an arrangement, and the action nowhere alleges that Hirabayashi does. Accordingly, applicant requests reconsideration and withdrawal of the rejection of claim 51 for the reasons discussed above with respect to claim 1. (Independent claim 21, which has not been individually rejected, similarly recites "a capacitance wiring formed so as to be in contact with the planarization insulating film," and is allowable for at least this reason.)

Claims 3-10, 13-20, 45, 49 and 52-58 have been rejected as being unpatentable over Hirabayashi in view of Sakuramoto.

With respect to claims 3-10, which depend from claim 1; claims 13-20, which depend from claim 11; claim 45, which depends from claim 43; claim 49, which depends from claim 47; and claims 52-54, which depend from claim 51, applicant requests reconsideration and withdrawal of this rejection because Sakuramoto does not remedy the failure of Hirabayashi to describe or suggest the subject matter of the independent claims from which they depend.

With respect to independent claim 55 and its dependent claims 56-58, applicant requests reconsideration and withdrawal of the rejection because neither Hirabayashi, Sakuramoto, nor any proper combination of the two describes or suggests forming a thin film transistor that is over a planarization insulating film, with the transistor including a gate electrode electrically connected to a lower layer wiring that is located under the planarization insulating film, as recited in claim 55. The rejection does not indicate where or how this aspect of claim 55 may be found in Hirabayashi or Sakuramoto, and applicant has been unable to find any such discussion in Hirabayashi or Sakuramoto. (Independent claim 32, which has not been individually rejected, similarly recites a thin film transistor having a gate electrode connected in the same way as is recited in claim 55, and is allowable for at least this reason.)

Applicant submits that all claims are in condition for allowance.

Enclosed is a $180 check for the Information Disclosure Statement fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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